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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,283	08/27/2003	Takayuki Kitazawa	031080	4445

23850 7590 08/04/2006

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
RUTLAND WALLIS, MICHAEL	

ART UNIT	PAPER NUMBER
2835	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,283	KITAZAWA ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/30/2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

112 2nd traversal

Applicant has responded to the previous 112 rejection of claim 8, hence the previous 112 rejection of claim 8 is withdrawn. With respect to claim 1 and 18 the phrase "cutting off all the switching transistors to the switching transistors when all of the switching transistors are in a non-selected sate" present in both independent claims is still deemed indefinite. A suggested amendment to claims 1 and 18 such as "cutting of all the switching transistors when all of the switching transistors are in a non-selected sate" would be considered a definite and clear. As applicant was failed to remove or amend the above cited indefinite language the previous rejection is maintained

Merit based Arguments

Applicant's arguments filed 06/15/2006 have been fully considered but they are not persuasive. Applicants allege the switching transistors shown in Hamase FETs 1-6 are never in the non-selected states. Applicant specifically points out Hamase discloses FETs which are laid out with complementary logic such that cutting off of FETS 1-3 corresponds to the conduction of FETs 4-6. The complementary nature of Hamase's

second output in relation to the operation of the first output is noted by the examiner, however is insufficient to overcome the rejection. As applied in the rejection switching transistors refers to the FETs 1-3 arranged in the transmission route A1 which corresponds to an input and an output and also shows the use of control bias circuitry as claimed. The claim does not require every switching transistor in the device only switching transistors connected to one of an input and an output. Therefore the switching transistors FETs 1-3 connected to OUT1 anticipates the limitations of claim 1, hence the rejection is maintained.

Applicant also provides arguments to claim 18 where applicant points out the series connection of FETs 1-3 and alleges a connection of the switching transistors to an input or an output is not made by the FETs of Hamase. A connection need not be made directly to the input; intervening circuit elements may be present. In this case the input current signal is transmitted equally to all the FETs when the FETs are conducting. When the FETs 1-3 are cutoff none of the switches are electrically connected, as it is an open circuit (the circuit from the input to OUT1) when the FETs are cutoff. Therefore a connection is made by the switching transistors to the input.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a control bias for cutting off all the switching transistors to the switching transistors when all of the switching transistors are in a non-selected state." It cannot be determined by the office what applicant intends by cutting off all of the switching transistors to the switching transistor.

Claim 18 recites a similar limitation "supplying a control bias for cutting off all the switching transistors to the switching transistors when all the switching transistors are in a non-selected state." Similarly it cannot be determined by the office what applicant intends by cutting off all of the switching transistors to the switching transistor.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 14 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hamase (JP Pub No. 2002135095).

The following rejections are based on the examiners best interpretation of claims 1 and 18.

With respect to claim 1 and 18 Hamase teaches a switching circuit (item 11) comprising: switching transistors (items 1, 2, 3) connected to an output terminal (see node out1) of the switching circuit; and a control bias supply circuit (resistor circuitry connected terminal VC1) that supplies a control bias for cutting off all the switching transistors when all of the switching transistors are in a non-selected state.

With respect to claim 2 and 14 Hamase teaches the control bias supply circuit supplies the control bias to a connection node (node connecting the gate terminal of transistors 1, 2 and 3 with VC1) via which the switching transistors are commonly connected and the common connection node is connected to a ground potential through a resistor (item R1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095).

With respect to claim 3 Hamase is silent on the origin or location of the VC1 signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input voltage signal used to be located outside of the switching circuit if it is held by applicant this is not the operation of Hamase.

With respect to claim 11 Hamase teaches at least three switching transistors (transistors 1,2 and 3), which are commonly connected to the output terminal of the switching circuit.

With respect to claim 22 Hamase teaches supplying the control bias having a first voltage value (ON voltage) when at least one of the switching transistors is in a selected state and supplying the control bias having a second voltage (off voltage) value different from the first voltage value when all the switching transistors are in the non-selected state.

Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095) in view of Yoshida et al. (U.S. Pat. No. 4,317,055)

With respect to claim 4 Hamase does not teach the use of a diode connected in a forward direction in which the voltage signal is applied. Yoshida teaches switching circuit where control bias circuitry comprises a diode in the forward bias direction (Fig. 13). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hamase to use a diode connected in a forward bias direction to protect the transistor.

With respect to claim 6 Hamase teaches the source of the transistor is connected to a connection node. Hamase does not teach the node is connected via which the

switching transistors are commonly connected, while the other one of the source and drain is connected to a ground potential through a capacitive element. Yoshida teaches connecting a common ground terminal to of switching transistors. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect the switching transistors to the ground terminal.

Claims 5, 7-9, 13 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095) in view of Matsunaga et al. (U.S. Pub. No. 20030016082)

With respect to claims 7-9 and 20-21 Hamase teaches the device of claim 1 as understood by the examiner, however Hamase does not teach the control bias varies the control voltage of the control bias circuitry. Matsunaga teaches the use of a control bias circuit, which teaches the capability of varying the voltage, supplied the voltage control terminals of switching transistors. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hamase to use a control bias circuit similar to that seen in Matsunaga in order to prevent excess current flow to the switching transistors.

With respect to claims 5,13, 19 Hamase teaches the device of claim 1. Hamase does not teach the use of MESFET in the control bias supply circuit. Matsunaga teaches the use of transistors in the bias control circuitry if it is held no transistors are to be connected to the VC1 terminal of Hamase. Hamase teaches the use of FETs. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a MESFET over another type of FET to increase the switching speed

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095) in view of Ayasli et al. (U.S. Pat. No. 5,012,123)

With respect to claim 12 Hamase does not teach the use of a shunt transistor connected to a source of a first one of the switching transistors, wherein a voltage signal applied to a gate of a second one of the switching transistors is applied to a gate of the shunt transistor. Ayasli teaches the use of a shunt resistor. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a shunt resistor reduce noise.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095) in view of Ayasli et al. (U.S. Pat. No. 5,012,123)

With respect to claim 15 Hamase does not teach ballast resistors, each of which is connected between a source and a drain of a corresponding one of the switching transistors. Ayasli teaches the use of ballast resistors see fig 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to in order to establish a biasing voltage source and drain of the switching transistor.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn D. Feild can be reached on 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LYNN FEILD
SUPERVISORY PATENT EXAMINER